Notice of Allowability	Application No.	Applicant(s)	
	09/829,046	OHBAYASHI, SHIGEKI	
	Examiner	Art Unit	
	Son L. Mai	2818	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *Petition for Consideration of Holding of Abandonment*.

2. ☒ The allowed claim(s) is/are *1-7*.

3. ☒ The drawings filed on *10 April 2001* are accepted by the Examiner.

4. ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☒ All b) ☐ Some* c) ☐ None of the:
      1. ☒ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

5. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

6. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

7. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☒ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☒ Information Disclosure Statements (PTO-1449 or PTO/SB/08), Paper No./Mail Date 2
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application (PTO-152)
6. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
7. ☐ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

Son Mai
Patent Examiner
Art Unit 2818

DETAILED ACTION

1. The Petition to Withdraw Holding of Abandonment is granted because the Office action 11-28-01 was not received by Applicant.

2. Claims 1-7 are allowed.

3. The following is an examiner's statement of reasons for allowance: The prior art of record fails to teach a static semiconductor memory device having T-type bit line structure using horizontal memory cells to reduce layout area and increase operating speed. The static semiconductor memory device comprises: a number M x N (M: integer not less than 2; N: integer not less than 2) of memory blocks each of which include a number 8 x M of horizontal memory cells arranged in eight rows by M columns and which are arrange in M rows by N columns, a word line provided corresponding to each memory cell row of each memory block, first and second bit lines provided in common for the number M of memory block rows so as to correspond to each memory cell column, first and second bit line signal input/output lines provided corresponding to each memory block and connected to the first and second bit lines of a predetermined pair of the corresponding M pairs of the first and second bit lines, respectively, first and second data input/output lines provided corresponding to each memory block row for inputting/outputting data of the corresponding memory block row, first and second power supply lines provided corresponding to each memory block row, a global word line provided corresponding to each memory block row for selecting the corresponding memory block row, a global column selecting line provided in common for the number 11 x N of memory blocks so as to correspond to each memory cell column for selecting

the corresponding memory cell column, a selection circuit responsive to an address signal for driving the word line, the global word line and the global column selecting line to select any one memory block of the number M x N of memory blocks and any one memory cell of the number 8 x M of memory cells belonging to the memory block, a write/read circuit for writing/reading data of the memory cell, an a gate circuit for coupling a memory cell selected by the selection circuit to the write/read circuit through the first and second bit lines, the first and second bit line signal input/output lines and the first and second data input/output lines, wherein in each memory block column, the M sets of the first and second bit line signal input/output lines, the first and second data input/output lines, the first and second power supply lines, the global word lines and the global column selecting line are arranged above the number M of memory blocks respectively, and extend in the same direction as that of the word line, each set of the first and second bit line signal input/output lines, the first and second data input/output lines, the first and second power supply lines and the global word lines and the global column selecting lines are arranged above eight memory cell rows included in the corresponding memory block, respectively, the first power supply line is arranged between the first and second bit line signal input/output lines and the first and second data input/output lines, and the global word line, and the second power supply line is arranged between the first and second bit line signal input/output lines and the first and second data input/output lines, and the global column selecting line.

4. Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably

accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Son L. Mai whose telephone number is 571-272-1786. The examiner can normally be reached on 8am to 6pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David Nelms can be reached on 571-272-1787. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

10-04-04

Son L. Mai
Primary Examiner
Art Unit 2818